Inelastic electron tunneling spectroscopy study of metal-oxide-semiconductor diodes based on high-κ gate dielectrics

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Inelastic electron tunneling spectroscopy (IETS) was applied to characterize the microstructure, interface, and trap-related states in silicon metal-oxide-semiconductor devices consisting of high-κ gate dielectrics HfO_2, Y_2O_3, and stacked HfO_2/Y_2O_3 bilayer by molecular beam epitaxy and atomic layer deposition under various heat treatments. Reproducible vibrational modes of monoclinic HfO_2 and cubic Y_2O_3 were identified from IETS spectra, along with phonon modes related to interfacial structures for a given metal-oxide-semiconductor fabrication process. A simple modeling was employed to analyze the trap related features in IETS spectra of stacked HfO_2/Y_2O_3 bilayers, and showed that most traps are located near the HfO_2/Y_2O_3 interface due to dissimilar charge distributions of two ionic oxides of different cation valences, and the presence of interfacial strains of dissimilar structures. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2831717]

Inelastic tunneling spectroscopy has been demonstrated over decades as a sensitive technique to detect the vibrational spectra of molecules in earlier metal-oxide-metal and later metal-oxide-semiconductor (MOS) tunneling junctions.[1–3] The characteristic phonon modes in inelastic electron tunneling spectroscopy (IETS) spectra are expected to provide valuable information about detailed bonding structure and chemical composition of high-κ gate oxides.[4,5] To effectively eliminate electrical shortcomings typical of high-κ dielectrics such as high density oxide trapped charges, interfacial traps, and mobility degradation, IETS technique was recently employed as a powerful means to reveal the origins of these defects.[5,6] Two kinds of traps may be identified from the IETS spectra, those contributed to the trap assisted conduction mechanism and those contributed to trapping in the gate dielectrics. Further, the polarity dependence of the IETS spectra has led to ascribe the phonon modes with respect to the lower and upper interfaces and to determine the approximate locations of traps within the gate dielectrics.[4–6]

In this study, we have employed IETS to probe a series of silicon MOS diodes consisting of high-κ HfO_2 ($\kappa \sim 15-18$), Y_2O_3 ($\kappa \sim 14-17$), and stacked HfO_2/Y_2O_3 bilayer as the gate dielectrics. We showed that IETS spectra obtained from MOS diodes made of HfO_2 prepared by various growth and processing conditions such as molecular beam epitaxy (MBE) and atomic layer deposition (ALD) revealed reproducible vibrational modes of monoclinic HfO_2 and cubic Y_2O_3, consistent with earlier Raman and infrared measurements.[7,8] Further, the presence of these phonon modes are closely related to dielectric microstructure and interfacial structure unique of a given MOS fabrication process. A simple modeling was employed to estimate the energy and physical location of the traps that appeared in the stacked HfO_2/Y_2O_3 bilayers, thus elucidating the nature of formation of these traps.[5,6]

The MOS diodes were fabricated on *n*-type, (100) silicon substrate with an arsenic dopant concentration as high as $2\times10^{19}/cm^3$ to ensure the Si substrates are sufficiently conducting when immersed in liquid nitrogen (77 K) or liquid helium (4.2 K) during IETS measurements. Postfurnace anneals in flowing gas stream were applied to most samples prepared by MBE and ALD. An aluminum gate electrode 300 nm thick was evaporated to complete the diode. The IETS spectra were obtained by taking the second derivatives of current-voltage curves by the standard lock-in technique at 4.2 K.[3] The dielectric thickness as calibrated by ellipsometry was kept around 3 nm to yield sufficiently large leakage, and strong second derivative d^2I/dV^2 signals. The individual thickness of HfO_2/Y_2O_3 stack was determined from x-ray reflectivity and cross sectional high resolution transmission electron microscopy (HRTEM).

By taking advantage of the bias polarity dependence of tunneling spectroscopy, the vibration modes were ascribed to be adjacent to the gate/dielectric interface or to the dielectric/Si interface.[4] Since the electrons have high probability to interact with the vibrational modes near the positively biased electrode, the IETS spectrum in electron substrate injection would reveal more information on Al/dielectrics interface, whereas the spectrum with electron gate injection would reveal more information on dielectrics/Si interface. Figure 1(a) is electron substrate injection (gate positively biased) IETS spectra of $Al/HfO_2/Si$ MOS diodes fabricated under various conditions and Fig. 1(b) is corresponding IETS spectra in electron gate injection (gate negatively biased). Reproducible and well defined vibrational modes of monoclinic HfO_2 in both spectra were identified, consistent with the published Raman and IETS data[7,8] as tabulated in Table I. In addition, the vibration modes of Hf silicate ($\sim$115 mV) and SiO_2 ($\sim$130–150 mV) were detected preferably in electron gate injection spectra. For instance, in the 600 °C N_2 annealed samples by ALD, strong Si–O bond features are signatures of inevitable formation of SiO_2 and Hf silicate near the HfO_2/Si interface inherent in such deposition method. Unlike the ALD case the MBE-

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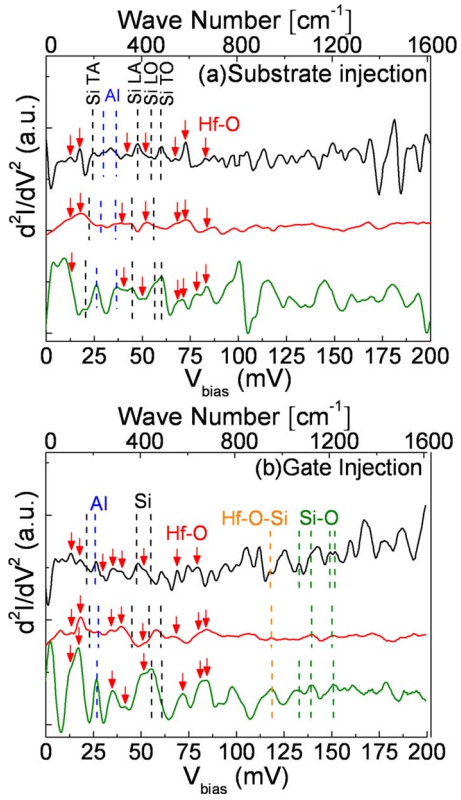

FIG. 1. (Color online) (a) Substrate injection and (b) gate injection IETS spectra of 600 °C N_2 annealed ALD-grown HfO_2 film (black line), 600 °C UHV annealed MBE-grown HfO_2 film (red line), and 600 °C N_2 annealed MBE-grown HfO_2 films (green line). The features of Si phonons appeared at 19 (TA), 44 (LA), 53 (LO), and 58 (TO) mV are denoted by black dotted lines, and the peaks associated with Hf–O bonds at 105, 146, 278, 319, 416, 555, 645, and 680 mV are denoted by red arrows. The peaks associated with Al, Hf–O–Si, and Si–O are denoted by blue, orange, and green dotted lines, respectively.

grown HfO_2 films annealed at 600 °C in ultrahigh vacuum showed rather weak features associated with SiO_2 vibrational modes, possibly due to the lack of oxygen during vacuum anneals, thus, preserving the atomically abrupt HfO_2/Si interface unique of the MBE growth.[9] The prominent features near 100 mV of the lower (MBE+600 °C N_2 annealing) spectrum and near the 175 mV of the upper (ALD+600 °C N_2 annealing) spectrum in Fig. 1(a) could be attributed to charge trapping features.[5,6]

Another high-κ dielectrics Y_2O_3 ($\kappa \sim 14-17$) is known to have small ionic polarizability leading to weaker phonon scattering and enhanced carrier mobility.[10,11] Its IETS spectra are shown in Fig. 2 and inset for MBE-grown films 3 nm thick annealed at 600 °C in furnace and 900 °C in rapid thermal processing (RTP), respectively. The intensity of Y_2O_3 vibrational modes in the former was quite weak compared to the Si phonon strength in the same spectrum. The marked increase in the intensity of Y_2O_3 phonons upon the 900 °C annealing may result from incipient recrystalization of Y_2O_3.[11] The peaks at 15, 30, 38, 46, 51, 65, 69, and 75 mV indicated by arrows were identified as the vibrational modes of cubic Y_2O_3 by referring to the data of Raman,[12] infrared,[13] and tunneling spectroscopies.[1] Furthermore, the broad peak appeared near 110–140 mV in the 900 °C spectrum but absent in the 600 °C spectrum is attributed to SiO_2 vibrational modes near the Y_2O_3/Si interface due to chemical reactions at 900 °C annealing.

TABLE I. Summary of vibrational frequencies of HfO_2 (in cm^{-1}) from measured IETS spectra in comparison with monoclinic HfO_2 (in cm^{-1}) published data from Raman (Ref. 7), and IETS (Ref. 4).

		ALD		MBE		MBE	
Raman of Kim	IETS of He	600 °C Gate	N_2 Sub	600 °C Gate	UHV Sub	600 °C Gate	N_2 Sub
112		105	100	107	100	103	105
134							
148		150	141	146	146	140	
165							
241							
254							
270	272	283		278		278	
324		319	334	319	320	328	324
336							
381							
398		416	416	416	411	412	402
496							
519							
550	568	555	548	555	552	578	552
577			584		584		575
639		640		645		649	634
670	660		666	681	675	680	671
773							

A bilayer dielectric structure consisting of HfO_2 (top) with Y_2O_3 (bottom) was further investigated. Surprisingly, the spectra of an Al/HfO_2 (1.7 nm)$/Y_2O_3$(1.4 nm)$/Si$ sample are dominated by series of symmetric, intense charge trapping features that first appeared after 400 °C N_2 annealing, then become very prominent after 600 °C N_2 annealing, as illustrated in Fig. 3. Based on a simple modeling, we are able to estimate both physical location and energy level of these traps as listed in Table II, where V_f and V_r are the voltages at which the trap feature occurs in forward biased (gate positive biased), and reverse biased (gate negative biased) spectra, and V_t is the energy level of traps at zero bias.[5,6] The effective electrical thickness of dielectrics (d_0), and the effective electrical distance (d_t) between the trap state and gate electrode are defined by $d_0 = \int_0^{x_0} 1/\varepsilon(x)dx$, and $d_t = \int_0^{x_t} 1/\varepsilon(x)dx$, where x_0 is total thickness of the dielectrics, and x_t is the distance between the trap and gate electrode.[5,6] The energy level of the trap is given by $V_t = V_f V_r/(V_f + V_r)$, and physical location of the trap is given by $d_t = d_0 V_f/(V_f + V_r)$.

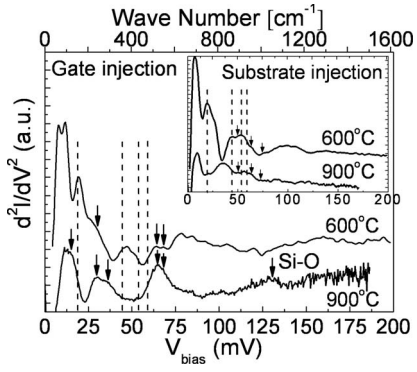

FIG. 2. IETS spectra (gate injection) of a MBE-grown Y_2O_3 annealed at 600 °C in furnace and 900 °C in RTP. The inset is substrate injection spectra with units the same as the main figure.

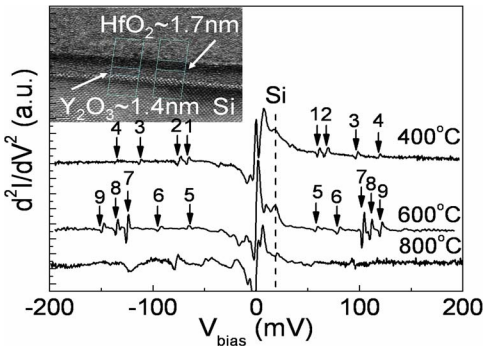

FIG. 3. (Color online) IETS spectra of an Al/HfO_2 (1.7 nm)$/Y_2O_3$ (1.4 nm)$/Si$ bilayer stack annealed at 400, 600, and 800 °C in N_2 for 3 min, respectively. The inset is a cross sectional HRTEM image showing the interfaces.

From the analysis, the d_t/d_0 ratio of most traps appeared in both 400 and 600 °C N_2 annealed samples are close to 0.45–0.47. Another bilayer of Al/HfO_2(1.2 nm)$/Y_2O_3$ (1.5 nm) with a different HfO_2 to Y_2O_3 thickness ratio was studied for comparison. The deduced d_t/d_0 ratio is again close to 0.45. Because the dielectrics constants of HfO_2 ($\varepsilon \sim 16-18$) and Y_2O_3 ($\varepsilon \sim 14-17$) (Refs. 10 and 11) are comparable, this implies that x_t/x_0 is ~0.5 in both cases. Given the thickness determination is subject to large uncertainties in very thin range, our analysis suggests that most traps in both bilayer stacks are located about the same distance with respect to the Al/HfO_2 interface, i.e., near the HfO_2/Y_2O_3 interface, as opposed to be near the Y_2O_3/Si interface.

TABLE II. The trap energy level (V_t) and the (d_t/d_0) ratio of the effective electrical distance (d_t) between the trap and the gate to the effective electrical thickness of dielectrics (d_0) for each trap-related state in Fig. 3.

Bilayer sample	Trap label	V_f (mV)	V_r (mV)	V_t (mV)	d_t/d_0
	1	60	66	31	0.47
HfO_2(1.7 nm)$/Y_2O_3$(1.4 nm)	2	67	75	35	0.47
400 °C	3	97	112	52	0.46
	4	118	135	63	0.46
	5	58	66	31	0.46
HfO_2(1.7 nm)$/Y_2O_3$(1.4 nm)	6	78	93	42	0.45
600 °C	7	103	124	56	0.45
	8	111	135	61	0.45
	9	120	148	66	0.45
	1	26	32	14.3	0.45
HfO_2(1.2 nm)$/Y_2O_3$(1.5 nm)	2	87	94	45.2	0.48
600 °C	3	99	108	51.7	0.48

In addition, the intense trap features suggest that the interface between these two oxides contains a significant defect concentration and the origin may have to do with the fact that the Y cation in Y_2O_3 is trivalent, and the Hf cation in HfO_2 is tetravalent, thus, leading to dissimilar charge distributions near the interface as likely sites for defects. The pronounced enhancement in intensity of the traps after the 600 °C annealing from the 400 °C annealing may be attributed to increased strains near the interface of dissimilar structures that Y_2O_3 remains to be amorphous, while HfO_2 is already recrystallized. Further, upon 800 °C annealing the trap features became much weaker, consistent with the reduction of strains due to diffusion/intermixing at 800 °C.

In summary, IETS was employed to study high-κ dielectrics HfO_2, Y_2O_3, and HfO_2/Y_2O_3 bilayer to extract the energies of vibrational modes in monoclinic HfO_2 and cubic Y_2O_3 phases with good reproducibility, and to further characterize the interfacial structure and chemical bonding unique of the MBE and ALD processes. By analyzing the salient features of charge trapping in IETS spectra of stacked HfO_2/Y_2O_3, we infer that these traps are located mostly near the interface between HfO_2 and Y_2O_3, likely caused by dissimilar charge distributions of two ionic oxides of different cation valences, and the presence of interfacial strains at dissimilar structures. Our work, thus, has raised an important possibility of tailoring the trap locations in a gate dielectric stack through multilayering a number of dielectric materials of dissimilar cation valences.

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